



INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	09/883,836
Filing Date	June 17, 2001
First Named Inventor	Bailey
Art Unit	2123
Examiner Name	

U.S. PATENT DOCUMENTS

NOTE: If this application was filed after June 30, 2003, copies of United States patents and United States published patent applications do not have to be provided to the Patent Office. This requirement of 37 C.F.R. § 1.98(a)(2)(i) has been waived by the United States Patent and Trademark Office pursuant to the Official Gazette Notice on August 5, 2003 (1276 OG 55).

Examiner's Initials*	Cite No. (optional)	Number	Publication Date	Name of Applicant or Patentee
THS		5,768,567	6.16.1998	Klein et al.

FOREIGN PATENT DOCUMENTS

Examiner's Initials*	Cite No. (optional)	Country	Number	Publication Date	Name of Applicant or Patentee
THS		Europe	EP 0 418 980	3.27.1991	

Examiner's Initials*	Cite No. (optional)	OTHER DOCUMENTS
THS		Harris et al., "The co-verification of an RTOS in an SOC," <i>Integrated System Design</i> , CMP Media Inc., USA, Vol. 13, No. 143, pp. 23-30 (May 2001).
THS		Shah et al., "Target processor and co-verification environment independent adapter--a technology to shorten cycle-time for retargeting TI processor simulators in HW/SW co-verification environments," ASIC/SOC Conference Proceedings, pp. 37-41 (September 1999).
THS		Yoo et al., "Fast hardware-software coverification by optimistic execution of real processor," Proceedings Design, Automation and Test in Europe Conference and Exhibition 2000, Proceedings of Meeting on Design Automation and Test in Europe, Paris, France, pp. 663-668 (March 2000).

EXAMINER
SIGNATURE:

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3/11/05

* Examiner: Initial if reference considered, whether or not in conformance with MPEP 609. Draw line through cite if not in conformance and not considered. Include copy of this form with next communication to applicant.